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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,568	10/24/2003	Patrick Lysaght	X-1374 US	1995

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,568	LYSAGHT ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/693,568, and RCE filed on 08/21/2006. Claims 1, 11, 14 and 17 have been amended. Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4 and 6-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Jyu et al. (U.S. Patent 5,880,967).

4. As to claims 1, 11, 14 and 17 Jyu teaches:

(1), (11), (14) A method/program/computer of designing an integrated circuit having a plurality of logic paths, comprising (col.5, ll.38-67, col.6, ll.1-3; col.30, ll.40-43):

designing the integrated circuit in accordance with timing constraint data (constraint file/delay limits/timing constraints; user needs to specify the timing constraints through the configuration command – col.11, 51-52) using a timing-driven design process (for example, in slack-driven mode, the goal is to make the slack values positive - col.11, ll.25-26; A positive slack value indicates the timing constraints of a circuit are satisfied while a negative value indicates these constraints are violated and transistor resizing is required - col.11, ll.31-33) to produce a design result optimized for timing performance (The execution report also includes the results of initial searching in

portion 2004. The initial circuit, scaling circuit and changing circuit are identified with the abbreviations "Initial," "S," and "C," respectively. In this case the scaling factor equals 0.5, and the smallest transistor size is 1.0 um. Since the changing circuit has the best slack value (i.e., +5.63), engine 320 selects this circuit as the initial circuit for transistor autosizing - col.27, ll.47-54, Fig. 20) and not for power consumption (In slack-driven mode, the goal is to make the slack values positive – col.11, ll.25-26; A positive slack value indicates the timing constraints of a circuit are satisfied while a negative value indicates these constraints are violated and transistor resizing is required – col.11, ll.31-33) (col.3, ll.43-47; col.7, ll.12-18; col.11, ll.25-64; col.19, ll.52-59; col.20, ll.23-33; col.27, ll.24-26; col.27, ll.40-57);

identifying any logic paths (circuit paths/paths) in said plurality of logic paths that have a timing characteristic within a threshold to define a first set of logic paths (other transistors which are not on the critical paths nor the possible critical paths – col.20, ll.52-53), where any logic paths in said plurality of logic paths other than said first set of logic paths define a second set of logic paths (The timing data 414b also identifies the critical path based on delay as well as slack – col.19, ll.58-59; only critical paths need to be shortened to improve the delay. The critical paths are the paths of which the delays are longer than a delay requirement (i.e., requirement set by the user). Different outputs can have different required times. Along the critical paths, the transistor sizes need to be increased. Increasing the transistor size can reduce the driving resistance, and therefore the delay of the critical paths. The new transistor sizes are computed from the criticality of the path, which is reflected by the path delay (or the slack value as

discussed below). Since some non-critical paths may drive the transistors on the critical paths, it is very likely that some originally non-critical paths will become critical after sizing up the transistors on the critical paths. In order to avoid deteriorating the delay of non-critical path too much, possible candidates for critical paths should also be addressed. These paths can be determined from the fanin of the critical path transistors and the path delays - col.20, ll.31-51) (col.3, ll.43-62; col.19, ll.52-59; col.20, ll.33-63; col.12, ll.28-30 Fig.7); and

selectively optimizing the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths (Once the slack values for all signals in a circuit become positive, engine 320 will try to minimize power - col.11, ll.47-48; In requirement mode, two requirement parameters may be specified: delay and power. If the delay requirement is specified, engine 320 will first satisfy the specified delay and then minimize the power - col.10, ll.56-59) (col.10, ll.56-59; col.11, ll.47-48);

(17) A method of designing an integrated circuit, comprising (col.30, ll.40-43):

designing the integrated circuit in accordance with timing constraint data (constraint file/delay limits/timing constraints; user needs to specify the timing constraints through the configuration command – col.11, 51-52) using a timing-driven design process (for example, in slack-driven mode, the goal is to make the slack values positive - col.11, ll.25-26; A positive slack value indicates the timing constraints of a circuit are satisfied while a negative value indicates these constraints are violated and transistor resizing is required - col.11, ll.31-33) to produce a design result optimized for

timing performance (The execution report also includes the results of initial searching in portion 2004. The initial circuit, scaling circuit and changing circuit are identified with the abbreviations "Initial," "S," and "C," respectively. In this case the scaling factor equals 0.5, and the smallest transistor size is 1.0 um. Since the changing circuit has the best slack value (i.e., +5.63), engine 320 selects this circuit as the initial circuit for transistor autosizing - col.27, ll.47-54, Fig. 20) and not for power consumption (In slack-driven mode, the goal is to make the slack values positive – col.11, ll.25-26; A positive slack value indicates the timing constraints of a circuit are satisfied while a negative value indicates these constraints are violated and transistor resizing is required – col.11, ll.31-33) (col.3, ll.43-47; col.7, ll.12-18; col.11, ll.25-64; col.19, ll.52-59; col.20, ll.23-33; col.27, ll.24-26; col.27, ll.40-57);

identifying timing critical logic circuitry (The timing data 414b also identifies the critical path based on delay as well as slack – col.19, ll.58-59; only critical paths need to be shortened to improve the delay. The critical paths are the paths of which the delays are longer than a delay requirement (i.e., requirement set by the user). Different outputs can have different required times. Along the critical paths, the transistor sizes need to be increased. Increasing the transistor size can reduce the driving resistance, and therefore the delay of the critical paths. The new transistor sizes are computed from the criticality of the path, which is reflected by the path delay (or the slack value as discussed below). Since some non-critical paths may drive the transistors on the critical paths, it is very likely that some originally non-critical paths will become critical after sizing up the transistors on the critical paths. In order to avoid deteriorating the delay of

non-critical path too much, possible candidates for critical paths should also be addressed. These paths can be determined from the fanin of the critical path transistors and the path delays - col.20, ll.31-51) (col.3, ll.43-62; col.19, ll.52-59; col.20, ll.33-63; col.12, ll.28-30 Fig.7); and

selectively optimizing the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths (Once the slack values for all signals in a circuit become positive, engine 320 will try to minimize power - col.11, ll.47-48; In requirement mode, two requirement parameters may be specified: delay and power. If the delay requirement is specified, engine 320 will first satisfy the specified delay and then minimize the power - col.10, ll.56-59) (col.10, ll.56-59; col.11, ll.47-48).

5. As to claims 2, 4, 6-10, 12-13, 15-16 and 18-20 Jyu recites:

(2), (12), (15), (18) The method/program/machine, wherein said selectively optimizing comprises power optimizing only said second set of logic paths (col.21, ll.1-50);

(4), (7), (13), (16), (19) The method/program/machine, wherein said selectively optimizing comprises power optimizing said first set of logic paths and said second set of logic paths (col.20, ll.13-63);

(6), (8) The method comprises rejecting a power optimization for each logic path in the third set of logic paths (col.26, ll.35-56);

(9) The method, wherein the threshold is defined by a percentage of parameter in the timing constraint data (col.26, ll.61-67; col.27, ll.1-20);

(10), (20) The method, wherein said threshold is defined by an absolute value (col.11, ll.25-64).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jyu in view of Chen (US Patent 6,687,888).

With respect to claims 3 and 5 Jyu teaches the features above but lacks a method of designing the integrated circuit having the plurality of logic paths, wherein power optimizing comprises placing first and second set of logic with respect to target device, and routing connections of said first and second set of logic paths.

As to claims 3 and 5 Chen discloses:

The method of designing the integrated circuit having the plurality of logic paths, wherein power optimizing comprises placing first and second set of logic with respect to target device, and routing connections of said first and second set of logic paths (col.4, ll.20-26; col.7, ll.19-57).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Chen's teaching regarding the method of designing the integrated circuit having the plurality of logic paths, wherein power optimizing comprises placing first and second set of logic with respect to target device, and routing

connections of said first an second set of logic paths and use it in Jyu's invention to improve optimization process by using place and routing tools thereby specifically increasing an efficiency of the integrated circuit design.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thuan Do
THUAN DO
Primary examiner
09/27/2006

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